UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,129	06/30/2003	Merritt Funk	071469-0304316	6686

909 7590 08/22/2005

PILLSBURY WINTHROP SHAW PITTMAN, LLP
P.O. BOX 10500
MCLEAN, VA 22102

EXAMINER	
KOSOWSKI, ALEXANDER J	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,129	FUNK, MERRITT	
	Examiner	Art Unit	
	Alexander J. Kosowski	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1) Claims 1-9, as amended 05/20/05, are presented for examination. This application is now an RCE. This is a non-final rejection.

Claim Rejections - 35 USC § 102

2) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3) Claims 1-6 and 8 are rejected under 35 U.S.C. 102(e) as being unpatentable by Hussey, Jr. et al (U.S. Pat 6,728,591).

Referring to claim 1, Hussey teaches a method of operating a semiconductor processing system comprising determining a first state and a second state for a wafer via optical digital profiling using critical dimension data and sidewall angle data (col. 7 lines 1-21 and col. 7 line 67 through col. 8 line 6, whereby measurements may be obtained after each of multiple processing steps of the wafers to determine multiple states); determining a process recipe to change the state of the wafer from the first state to the second state and performing the process recipe on the wafer, wherein the state of the wafer changes from the first state to a processed state (col. 7 lines 35-59), determining when the processed state is not the second state and updating the process recipe (col. 7 line 50 through col. 8 line 6).

Referring to claims 2-3, Hussey that the determining of the first state further comprises measuring and receiving data from at least one of an electrical property and a physical property (col. 7 lines 1-21).

Referring to claims 4-5, Hussey teaches that the determining of the second state further comprises measuring and receiving data from at least one of an electrical property and a physical property (col. 7 lines 1-21).

Referring to claim 6, Hussey teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the process recipe comprises feeding forward at least one process recipe based on the first and second state of the wafer (col. 7 line 50 through col. 8 line 6).

Referring to claim 8, Hussey teaches the method of operating a semiconductor processing system as claimed in claim 1, further comprising: determining differences between the processed state and the second state and feeding back the differences (col. 7 lines 50-66).

Claim Rejections - 35 USC § 103

4) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5) Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussey, further in view of Reiss (USPGPUB 2003/0014145).

Referring to claim 7, Hussey teaches the method above. However, Hussey does not explicitly teach that determining the process recipe comprises predicting the second state using the first state of the wafer and a process model based on the process conditions.

Reiss teaches a method of operating a semiconductor processing system whereby a predicted state for a wafer being processed is determined and utilized to adjust the process recipe (Paragraphs 0047-0049).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to determine a predicted state and to utilize the prediction to adjust the process recipe taught by Hussey above since this would allow for target wafer properties to be determined (Reiss, Paragraph 0049), which would allow for more efficient processing of wafers and would allow a processing system to address both process drifts and fault conditions (Reiss, Paragraph 0011).

Referring to claim 9, Hussey teaches a method of operating a semiconductor processing system comprising determining a first and second state for a wafer via optical digital profiling using critical dimension data and sidewall angle data (col. 7 lines 1-21 and col. 7 line 67 through col. 8 line 6, whereby measurements may be obtained after each of multiple processing steps of the wafers to determine multiple states), determining a measured state for the wafer (col. 7 lines 1-21), and determining a recipe for changing the wafer state to the second state using the first state and the measured state (col. 7 lines 35-59). However, Hussey does not explicitly teach determining a predicted state for the wafer, wherein a predicted process recipe is used to change the state of the wafer from the first state to the predicted state, determining a modeled state for

the wafer, wherein a process model is used to change the state of the wafer from the first state to the modeled state, nor that determining the recipe is also based on these two states.

Reiss teaches a method of operating a semiconductor processing system whereby a modeled state and a predicted state for a wafer being processed are determined and utilized to adjust the process recipe (Paragraphs 0047-0049).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to determine a predicted state as well as a modeled state and to utilize these to adjust the process recipe taught by Hussey above since this would allow for target wafer properties to be determined (Reiss, Paragraph 0049), which would allow for more efficient processing of wafers and would allow a processing system to address both process drifts and fault conditions (Reiss, Paragraph 0011).

Conclusion

6) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander J Kosowski whose telephone number is 571-272-3744. The examiner can normally be reached on Monday through Friday, alternating Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. In addition, the examiner's RightFAX number is 571-273-3744.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Alexander J. Kosowski
Patent Examiner
Art Unit 2125

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100